UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,227	09/26/2001	Jerome Tsu-Rong Chu	42022/MJM/A717	1865

23363 7590 05/02/2003

CHRISTIE, PARKER & HALE, LLP
350 WEST COLORADO BOULEVARD
SUITE 500
PASADENA, CA 91105

EXAMINER
VOCKRODT, JEFF B

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/964,227	Applicant(s) CHU ET AL.	
	Examiner Jeff Vockrodt	Art Unit 2822	

-- Th MAILING DATE of this communication app ars on the cover she t with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19,27 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19,27 and 28* is/are allowed.

6)☒ Claim(s) *1-10,12,13 and 15-18* is/are rejected.

7)☒ Claim(s) *11 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This office action is in response to the amendment filed on March 4, 2003. Claims 1-19, 27, and 28 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 15-16, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 5,904,575 ("Ishida").

Ishida teaches a method of selectively incorporating nitrogen to affect differential oxide growth within a programming junction of an EEPROM device. Ishida replaces the conventional multi-mask oxidation programming junctions (PRJ) 110b for EEPROM with a single oxidation step that forms two oxide thickness 174, 130b and 172, 103c (Figs. 1-3; Figs. 9 and 15).

Claim 1 reads on Ishida as follows: providing a semiconductor substrate 102; introducing n-type impurities to form a programming junction 110b (Fig. 2); introducing nitrogen into a portion of the programming junction 110b (compare Figs. 9 and 15 with Figs. 1-3; the inhibited region 174 of Fig. 15 corresponds to region 130b of Fig. 1, which is where a masking step was required in conventional EEPROM processes as shown in Fig. 3); after introducing nitrogen into region 170, the substrate is annealed to form a thin oxide 174 and a thick oxide 172 in a single oxidation step (Fig. 9); and forming a capacitor (110a, 130b, 106a; Fig. 1). The essential elements of a mos capacitor are a diffusion region serving as a lower electrode, a capacitor dielectric on the substrate, and an upper electrode on the capacitor dielectric. These essential elements are shown in Fig. 1 whereas region 110a is a diffusion region serving as a lower

electrode; the tunnel oxide 130b (which has inhibited growth due to nitride implantation) is a dielectric; and the floating gate 106a is an upper electrode.

Claim 2. The programming junction of an EEPROM is a low capacitor electrode while the floating gate forms the upper electrode with a tunneling oxide in between. It is the tunneling oxide that Ishida is concerned with.

Claims 3 and 19. Ishida uses GILD to introduce nitrogen in the preferred embodiment but clearly teaches that implantation could be used to place nitrogen selectively within the junction. Ishida, col. 6, ll. 12-27. Claim 19, the top capacitor plate or floating gate 106b of the EEPROM of Fig. 1 must be a conductor otherwise it will not work.

Claim 15. The region under thick oxide 172 has no nitrogen, while the region under thin oxide 174 has nitrogen.

Claim 16. The substrate 102 is silicon and its oxide 172, 174 is silicon oxide.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 15-16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,904,575 ("Ishida") in view of U.S. Pat. No. 6.255,169 ("Li '169").

Ishida teaches a method of selectively incorporating nitrogen to affect differential oxide growth within a programming junction of an EEPROM device. Ishida replaces the conventional multi-mask oxidation programming junctions (PRJ) 110b for EEPROM with a single oxidation step that forms two oxide thickness 174, 130b and 172, 103c (Figs. 1-3; Figs. 9 and 15).

Claim 1 corresponds to Ishida as follows: providing a semiconductor substrate 102; introducing n-type impurities to form a programming junction 110b (Fig. 2); introducing nitrogen into a portion of the programming junction 110b (compare Figs. 9 and 15 with Figs. 1-3; the inhibited region 174 of Fig. 15 corresponds to region 130b of Fig. 1, which is where a masking step was required in conventional EEPROM processes as shown in Fig. 3); after introducing nitrogen into region 170, the substrate is annealed to form a thin oxide 174 and a thick oxide 172 in a single oxidation step (Fig. 9). Ishida forms tunnel oxide regions in an EEPROM, however, assuming that capacitors are not inherently formed by Ishida, claim 1 differs by requiring a capacitor and top capacitor plate.

Li '169 teaches a process for fabricating an EEPROM device that includes nitrogen implantation under the tunnel oxide region. More importantly, Li '169 teaches that stress-induced-leakage current can be measured by forming the tunnel oxide structure into a MOS capacitor (col. 6, ll. 23-54).

Li '169 and Ishida are closely related as methods of forming tunnel oxide regions of EEPROM devices.

It would have been obvious to one of ordinary skill in the art to at the time of the invention to form the tunnel oxide structures of Ishida into MOS capacitors. One of ordinary skill would have been motivated to form MOS capacitors from the tunnel oxide structures of Ishida in order to test the stress induced leakage current of the tunnel oxide layers as taught by Li '169.

Claim 2. The programming junction of an EEPROM is a low capacitor electrode while the floating gate forms the upper electrode with a tunneling oxide in between. It is the tunneling oxide that Ishida is concerned with.

Claims 3 and 19. Ishida uses GILD to introduce nitrogen in the preferred embodiment but clearly teaches that implantation could be used to place nitrogen selectively within the

junction. Ishida, col. 6, ll. 12-27. Claim 19, the top capacitor plate or floating gate 106b of the EEPROM of Fig. 1 must be a conductor otherwise it will not work.

Claim 15. The region under thick oxide 172 has no nitrogen, while the region under thin oxide 174 has nitrogen.

Claim 16. The substrate 102 is silicon and its oxide 172, 174 is silicon oxide.

Claims 5, 7, 9, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida and Li '169 as applied to claims 1-3, 15-16, and 19 above, further in view of U.S. Pat. No. 5,854,114 ("Li").

Ishida teaches a method of selectively incorporating nitrogen to affect differential oxide growth within a programming junction of an EEPROM device as discussed above. Ishida does not teach the claimed implant dose corresponding to the PRJ implant.

Li teaches a EEPROM cell similar to the EEPROM cell of Ishida's Figs. 1-3. Li teaches the EEPROM cell in more detail. Claims 7 and 13. Li teaches a PRJ implant of phosphorous with a dose of about $1x10^{14}$ to $1x10^{16}$ ions/cm^2 and an energy of 50-100 KeV. (Li, paragraph bridging cols. 4-5.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a dose of about $1x10^{14}$ to $1x10^{16}$ ions/cm^2 and an energy of 50-100 KeV to form the PRJ region of Ishida because these values are known for producing PRJ regions as taught by Li.

Claims 9 and 18 are met by the tunneling oxides grown simultaneously with the thin tunneling oxide 154 in (relatively) undoped portions of the substrate (Figs. 3l-3m).

Claims 5, 6, 12, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida and Li '169 as applied to claims 1-3, 15-16, and 19 above, further in view of U.S. Pat. No. 5,750,428 ("Chang").

Ishida teaches a method of selectively incorporating nitrogen to affect differential oxide growth within a programming junction of an EEPROM device as discussed above. Ishida teaches that the thin oxide is approximately 80-100 Angstroms while the thick oxide is approximately 140-180 angstroms. Ishida, col. 8, ll. 42-55. These ranges overlap the range wherein the thin oxide is less than 50% the thickness of the thick oxide. This substantial overlap between the claims and the prior art renders the claims prima facie obvious, particularly since there are no unexpected results for the oxide thickness. Additionally, with respect to claims 5, 6, 17, Chang teaches a non-volatile gate with a differentially grown oxide layer wherein the tunnel oxide is 50-100 angstroms and the gate oxide is 150-350 angstroms.

It would have been obvious to one of ordinary skill in the art at the time of the invention to form a tunnel oxide having a thickness of less than 55 angstroms and a gate oxide of 150 angstroms in the process of Ishida because these thickness were well known for EEPROM tunneling and gate oxides as taught by Chang.

Claim 12 requires oxidizing with a temperature range of 750°C-950°C (Ishida teaches 900°C, col. 8, ll. 42-48) for a time ranging from 5 to 15 minutes (Ishida does not disclose the time). Since these parameters together determine an oxide thickness that is met by Ishida the temperature is obvious in view of Ishida. 7

Claims 4, 8, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida and Li '169 as applied to claims 1-3, 15-16, and 19 above, further in view of U.S. Pat. No. 5,942,780 ("Barsan").

Ishida teaches a method of selectively incorporating nitrogen to affect differential oxide growth within a programming junction of an EEPROM device as discussed above. Ishida teaches that nitrogen implantation was known but does not disclose a mask for use with

nitrogen implantation and does not teach the claimed implantation parameters for the nitrogen implant.

Claims 4 and 8. Barsan teaches a nitrogen implant dose of $15x10^{14}/cm^2$ at a range of 29-32 KeV effective to suppress oxide growth. (Barsan, paragraph bridging cols. 7-8). The difference between claim 4 is that the implant dose for nitrogen is claimed as 5-9 KeV while Barsan additionally teaches optimizing the implant to minimize implant induced damage. It would have been obvious to one of ordinary skill in the art at the time of the invention to lower the implant energy of Barsan to within 5-9 KeV so as to minimize implant damage as taught by Barsan.

Claim 10. Barsan teaches using a photoresist to mask a nitrogen implant for the purpose of suppressing oxide growth in an EEPROM device. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a photoresist as an implant mask for nitrogen in the process of Ishida because Barsan teaches that photoresist were well known for masking nitrogen implants.

Allowable Subject Matter

Claims 19 and 27-28 are allowed.

Claims 11 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 11 and 14 were indicated allowable in the office action mailed November 4, 2002. Claims 27 and 28 are identical to previously allowed claims 11 and 14 and are thus allowable. Claim 19 is allowable as it depends from allowed claim 28. Claims 11 and 14 remain dependent from claim 1 and allowable as claim 1 was only narrowed by the amendment filed March 4, 2003.

Response to Arguments

Applicant's arguments apply only to the newly amended claim 1 and claims that depend therefrom. Applicant's amendment of claim 1 necessitated the examiner's new search and finding of U.S. Pat. No. 6,255,169 which would motivate one of ordinary skill to form a test capacitor from a tunnel oxide structure.

The rejection base on Ishida is maintained because Fig. 1 of Ishida inherently teaches a capacitor. The essential elements of a mos capacitor are a diffusion region serving as a lower electrode, a capacitor dielectric on the substrate, and an upper electrode on the capacitor dielectric. These essential elements are shown in Fig. 1 whereas region 110a is a diffusion region serving as a lower electrode; the tunnel oxide 130b (which has inhibited growth due to nitride implantation) is a dielectric; and the floating gate 106a is an upper electrode. I notice that applicant's inherency argument has not compared this particular aspect of Ishida with the claims. My understanding of applicant's argument is as follows: since tunnel oxide structures exist that do not necessarily result in a capacitor structure (no evidence is given by applicant to support this assertion), then Ishida does not inherently teach a capacitor structure. While the teaching of Ishida relating to nitrogen implantation could be applied to other EEPROM tunnel oxide structures besides the one shown in Fig. 1, it is unclear how this would negate the fact that the particular EEPROM structure shown in Ishida will necessarily result in a capacitor structure. The examiner submits that if there are any embodiments of Ishida's disclosure that necessarily result in the claimed capacitor structure, then the claims are anticipated under established principles of inherency. Of course, the fact that Ishida does not characterize certain portions of the EEPROM as "capacitor" is of little relevance to the inherency analysis since such express characterizations would obviate the need for an inherency analysis altogether.

Alternatively, if Ishida does not anticipate claim 1 under inherency principles, then it would have been obvious to form capacitor structures from the tunnel oxide structures taught by

Ishida in order to measure the stress-induced-leakage current of the tunnel oxides as taught by Li '169.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (703) 306-9144 who can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (703) 308-4905.

The fax numbers for this Group are (703) 305-3432, (703) 308-7722, (703) 305-3431, and (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

April 28, 2003
J. Vockrodt

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800